Product Flyer

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Version 2.05

MB86683B

Network Termination Controller (NTC)

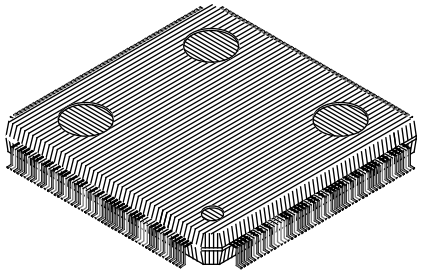
FML/NPD/NTC/FL/1204

The Fujitsu MB86683B is a highly integrated termination controller for broadband ATM networks.

The device implements transmission convergence functions associated with physical media based on SONET (155/51 Mbps), SDH (155 Mbps), DS3 (44 Mbps), E3 (34 Mbps) and unframed protocols. It includes a generic 8-bit parallel interface to an external transceiver, which is required only to provide serial / parallel conversion, and clock recovery.

The NTC is ideally suited to applications in ATM adapter cards and hubs. It can be used for UNI or NNI connections and conforms to the relevant ATM Forum, ANSI and ITU specifications.

PLASTIC PACKAGE
SQFP-176



FEATURES

- Implements TC sublayer functions associated with physical media based on SONET (SDH), DS3, E3 and cell based.
- Directly connects to external transceivers via a 20MHz 8-bit parallel interface.
- Implements framed OAM functions for F1/F2/F3 flows.
- Supports F4/F5 OAM cell insertion / extraction.
- Maintains statistics for all active virtual circuits, including cell and error counts, and OAM statistics.
- On-chip DMA controller for high speed transfer of statistics and inserted/extracted cells to/from system memory.
- Connects directly to the MB86689A Address Translation Controller (ATC) in order to provide real-time address translation in both directions.
- Microprocessor interface compatible with Motorola and Intel families of 16 and 32 bit processors.
- JTAG pins compliant to IEEE1149.1 are provided.
- Utopia Level 1 v2.01 compliant.
- Fabricated in 0.8 micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

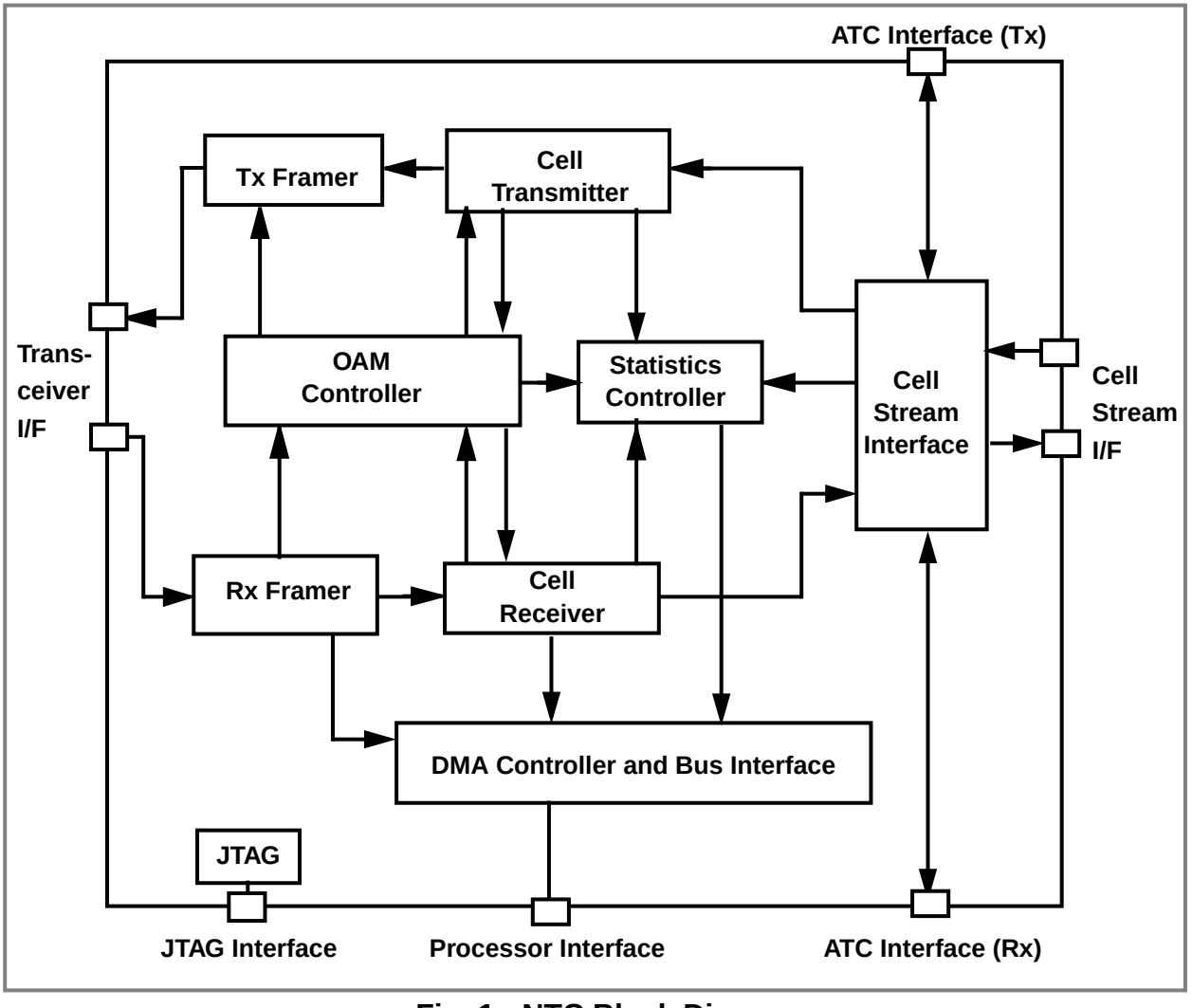


Fig. 1 - NTC Block Diagram

General

The NTC is a full-duplex device suitable to provide broadband termination functions. Address translation operates in conjunction with the MB86689A Address Translation Controller (ATC) allowing full flexibility for changing the VPI/VCI values at either end of the link. An internal RAM maintains a statistics record of VPI/VCI connections. The DMA controller points cells to be inserted/extracted from/to system memory in both the transmit and receive directions. Fig. 1 shows a logical block diagram of the NTC and Fig. 2 illustrates how the NTC might be used at system level.

Framers

The transmit and receive framers perform transmission convergence sub-layer functions with physical media based upon SONET (155/51 Mbps), SDH (155Mbps), DS3 (44Mbps) and E3 (34Mbps). An unframed mode of operation enables a transparent link to be established between the transceiver interface and the cell transmitter/receiver module.

Cell Handlers

Both the cell receiver and cell transmitter perform cell operations in accordance with ITU-T 1.432. The cell receiver performs the following functions:

- cell delineation
- cell header error detection and correction
- cell type recognition
- CRC-10 checking (for OAM cells)
- cell insertion/extraction via DMA
- cell discard.

The cell transmitter is responsible for providing the inverse functions to those of the cell receiver.

Cell Stream Interface

This interface passes ATM cells in the receive direction between the cell receiver and an external ATM layer device and vice-versa in the transmit direction. The Cell Stream Interface provides buffering of 9.85 cells to absorb delay when performing address translation. The CSI also supports Level 1 Utopia operation.

OAM Controller

The Operations, Administration and Maintenance (OAM) controller is responsible for providing support for error and performance monitoring for each of the framed modes of operation. Various received performance/error conditions within the receive framer may be passed to the transmit framer for inclusion in outgoing frames.

Network Statistics

The Network Statistics Controller maintains a record of events in a network statistics record (NSR), which is maintained in internal RAM. The NSR will be transferred to system memory by DMA under various control conditions. The NSR maintains statistics on up to 32 VP/VC connections simultaneously and records the total number of cells transmitted/received over the UNI.

DMA Controller

This allows data to be transferred between the NTC and system memory at high speed without the need for processor intervention. The controller supports five channels: Network Statistics, Cell Receiver Cell Extract, Cell Receiver Cell Insert, Cell Transmitter Cell Extract and Cell Transmitter Cell Insert.

Processor Interface

This interface has two functions. Firstly, it acts as an asynchronous slave for microprocessor access to NTC internal registers and secondly, it acts as an asynchronous master for DMA transfer of data between the NTC and system memory. This interface is configurable to be compatible with 16/32 bit Motorola/Intel systems.

JTAG

The NTC provides boundary scan test circuitry fully compliant with IEEE 1149.1 (JTAG).The NTC's JTAG circuitry permits easier board level testing to be carried out by allowing the signal pins on the device to form a serial scan chain around the device. JTAG test modes are controlled by accessing an internal test access port controller, which is in turn controlled by the 4 provided test access ports.

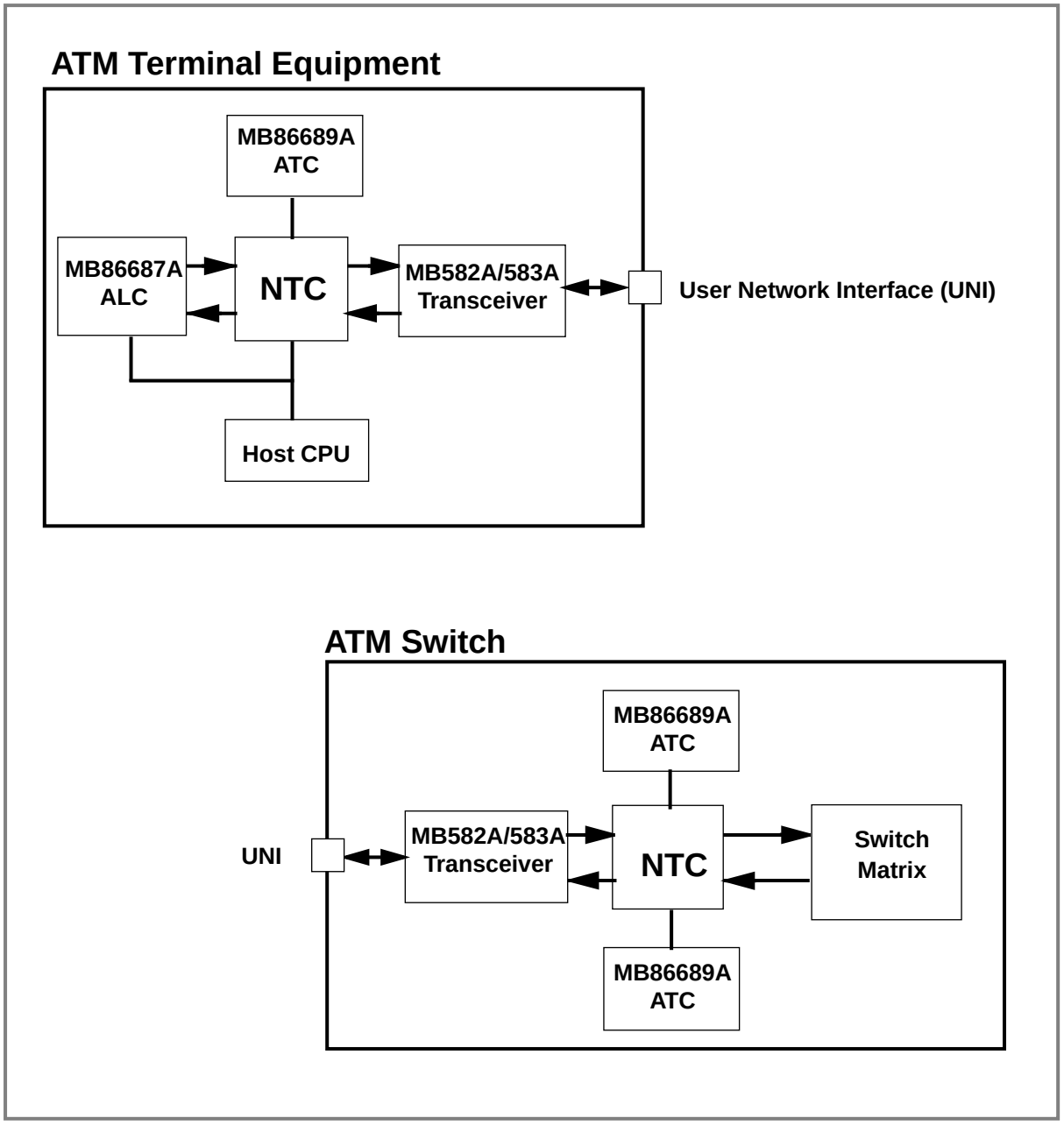


Fig. 2 - Example Configurations

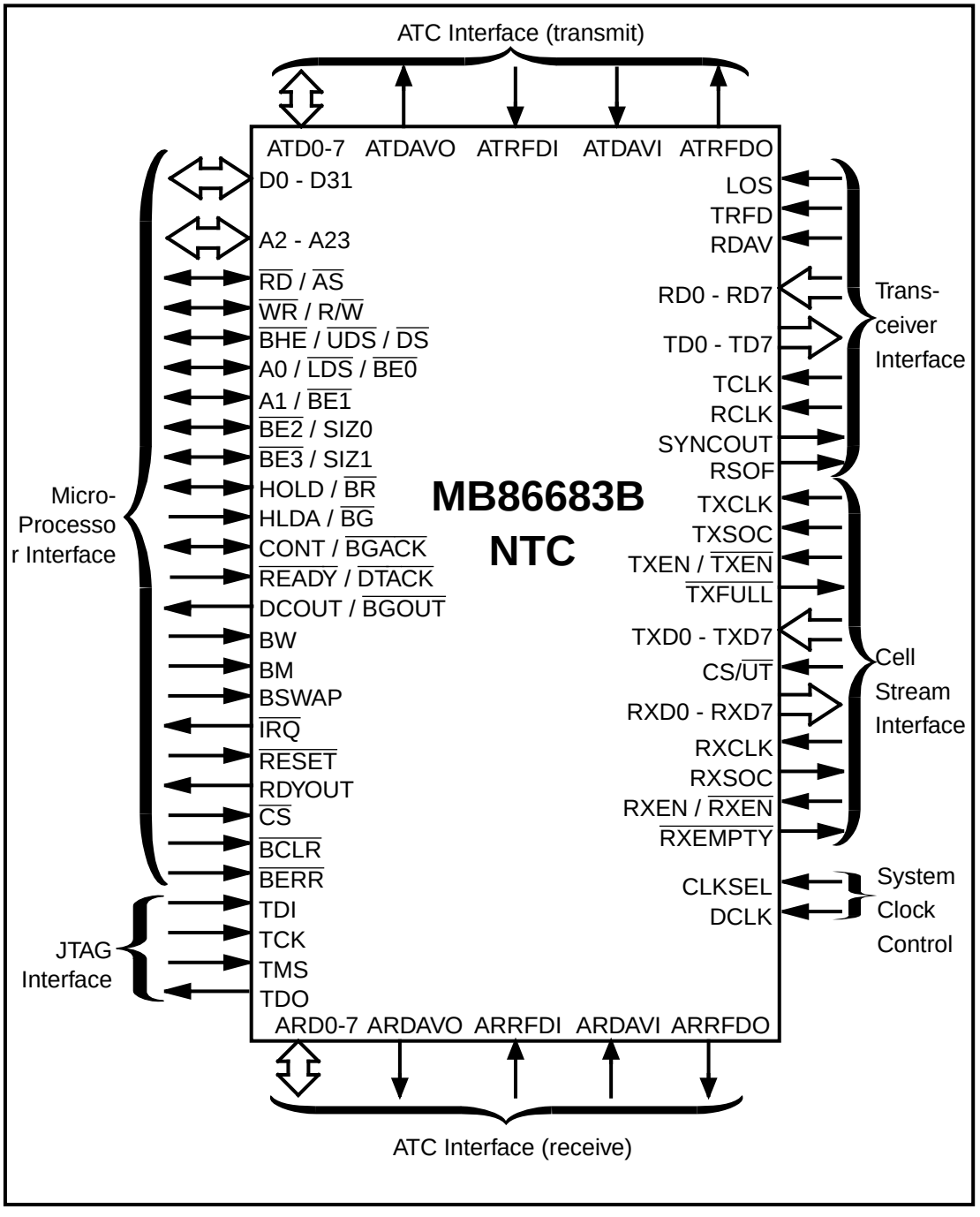


Fig. 3 - MB86683B I/O Block Diagram

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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