Chapter 2
L64711 Encoder Architecture

This chapter describes the architecture of the L64711 Reed-Solomon encoder chip from LSI Logic. An architectural overview is presented first. The overview is followed by specific descriptions of the encoding characteristics of the L64711. This chapter has the following five sections:

- Section 2.1, "L64711 Encoder Architecture"
- Section 2.2, "Codeword Waveforms"
- Section 2.3, "Channel Rate and Latency"
- Section 2.4, "Check Bytes"
- Section 2.5, "Summary"

2.1 L64711 Encoder Architecture

This section describes the architecture of the LSI Logic L64711 encoder. The three decoders that can be used with the L64711 are described later in this manual.

The implemented RS code in the encoder has the following generator polynomial:

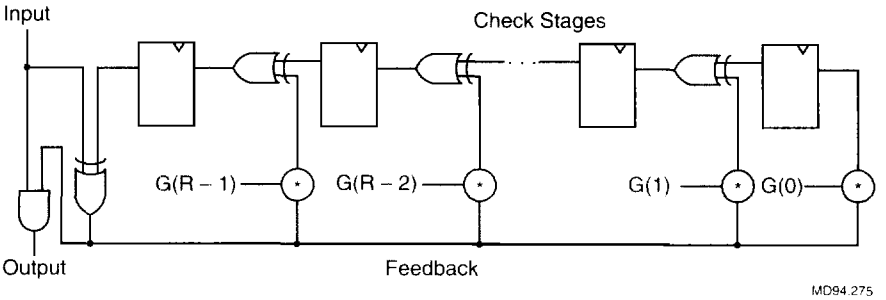
$$g(x) = \prod_{i=0}^{CB-1} \left(x + \alpha^{i} \right)$$

where α is a root of the binary primitive polynomial and the redundancy (CB) is a value from 2 to 32. The check polynomial, C(x), is the remainder of the message polynomial, M(x), multiplied by x^{CB} and divided by the generator polynomial, g(x) as expressed in the equation:

$C(x) = M(x)\ x^{CB}$ modulo $g(x)$.

Figure 2.1 shows a simplified schematic of the L64711 encoder.

Figure 2.1
Simplified Encoder Schematic

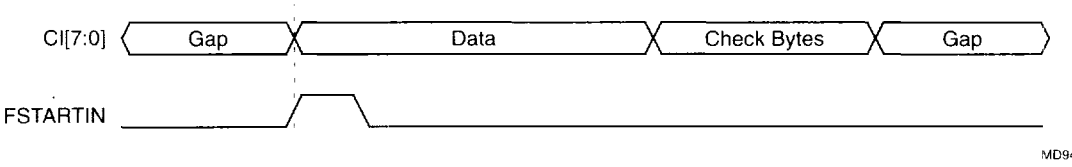


An R-stage, m-bit shift register implements the polynomial division in the encoding process. Between any two consecutive stages, a set of m exclusive-or gates implements finite field addition. The critical path of the encoder design involves the feedback path, which is broadcast to a set of CB finite field constant multipliers. The result is a set of K message bytes with appended CB check bytes. Correction power (t) is in the range 1 to $\left\lfloor \frac{CB}{2} \right\rfloor$.

2.2 Codeword Waveforms

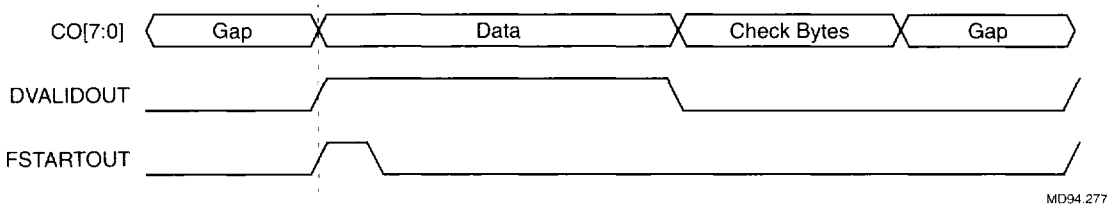
The following diagrams show timing signals related to the L64711 generated codeword. Note in Figure 2.2 that FSTARTIN causes the L64711 to accept the incoming data message. For the encoder, FSTARTIN should last one byte clock cycle or a maximum of eight bit-clock cycles. The gap time between the check bytes and the next FSTARTIN can be zero or any integer multiple of 8-bit bytes.

Figure 2.2
Encoder Data In



In Figure 2.3, two additional signals, DVALIDOUT and FSTARTOUT, provide the timing for the codeword to enter the transmission channel correctly.

Figure 2.3
Encoder Valid Data Out



2.3 Channel Rate and Latency

Input and output channel data may be either bit serial or symbol (byte) parallel. The maximum channel rate for the L64711 is 50 Mbits/s. Latency is a function of the L64711 output format as shown in Table 2.1.

Table 2.1
L64711 Latency

Check Bytes (CB)	Input/Output Format	Latency Bit Clock Cycles	Latency Symbol Clock Cycles
2 to 32	Serial in/Serial out	27	NA
	Serial in/Parallel out	27	NA
	Parallel in/Parallel out	19	5
	Parallel in/Serial out	19	NA

2.4 Check Bytes

The number of check bytes generated by the encoder or processed by each decoder is shown in Table 2.2

Table 2.2
Check Bytes per Codeword

Encoder	Check Bytes (CB)	Decoders	Check Bytes (CB)
L64711	2 to 32	L64712	2 to 10
		L64713	2 to 20
		L64714	2 to 32

2.5 Summary

Together, the family of encoder and decoder chips are designed for systems with transfer rates up to 50 Mbits/s. They are ideally suited to transmit digital television and radio signals over microwave or cable. Other applications with similar channel characteristics and data rates are also possible. Since the digital TV and radio markets are cost sensitive, the ECC chips from LSI Logic are optimized for low cost integration into embedded systems. In addition, the LSI Logic chips allow direct connection to LSI Logic's MPEG video and audio digital decoders in bit serial mode.